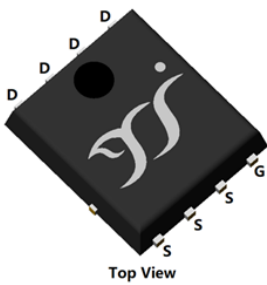
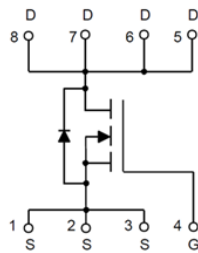
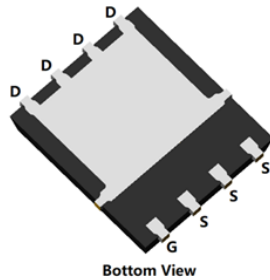


N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L



Product Summary

- V_{DS} 80V
- I_D 100A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 4.5mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- Battery protection
- Load switch
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	80	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ C$	I_D	100	A
	$T_C=100^\circ C$		63	
Pulsed Drain Current ^A		I_{DM}	400	A
Avalanche energy ^B		E_{AS}	600	mJ
Total Power Dissipation ^C	$T_C=25^\circ C$	P_D	152	W
	$T_C=100^\circ C$		61	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Limit	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10S$	$R_{\theta JA}$	22.3	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		40.7	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.819	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG100G08A	F1	YJG100G08A	5000	10000	100000	13" reel



YJG100G08A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	80	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	3.6	4.5	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	0.8	1.2	V
Maximum Body-Diode Continuous Current	I _S		-	-	100	A
Gate resistance	R _G	f=1MHz, Open drain	-	2	-	Ω
Transconductance	G _{fs}	V _{DS} =10V, I _D =50A		71.5		S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =40V, V _{GS} =0V, f=1MHz	-	5666	-	pF
Output Capacitance	C _{oss}		-	860	-	
Reverse Transfer Capacitance	C _{rss}		-	7.5	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{DS} =40V, V _{GS} =10V, I _D =50A	-	73	-	nC
Gate-Source Charge	Q _{gs}		-	25	-	
Gate-Drain Charge	Q _{gd}		-	12	-	
Reverse Recovery Charge	Q _{rr}	I _F =50A, di/dt=100A/us	-	50	-	ns
Reverse Recovery Time	t _{rr}		-	44	-	
Turn-on Delay Time	t _{D(on)}	V _{DS} =40V, V _{GS} =10V, R _G =3Ω, I _D =50A	-	27	-	ns
Turn-on Rise Time	t _r		-	32	-	
Turn-off Delay Time	t _{D(off)}		-	54	-	
Turn-off fall Time	t _f		-	17	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=50V, V_{GS}=10V, L=3mH I_{as}=20A.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C.



■ Typical Performance Characteristics

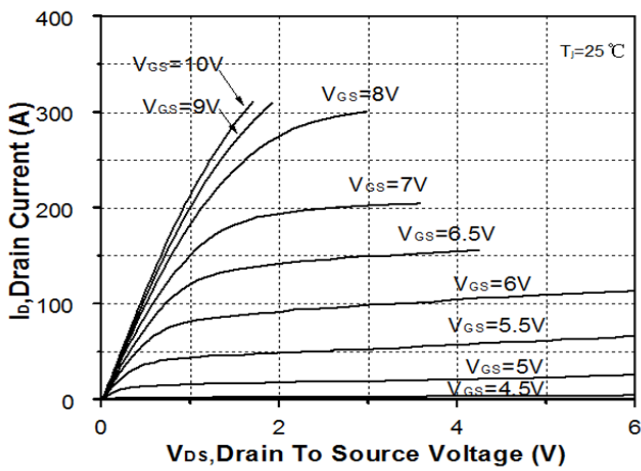


Figure1. Output Characteristics

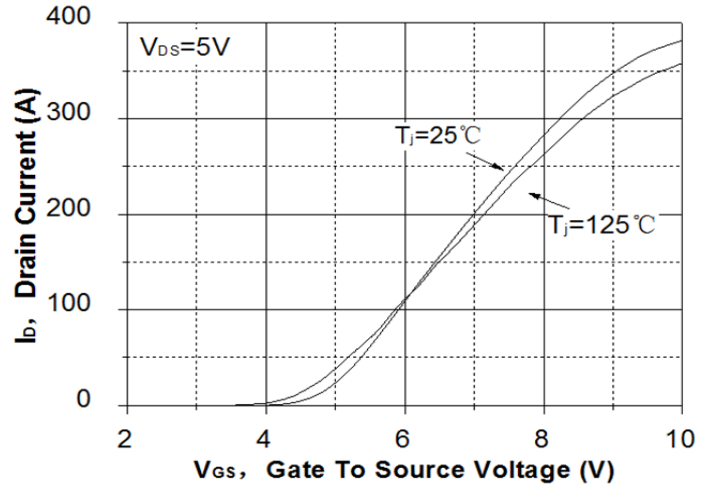


Figure2. Transfer Characteristics

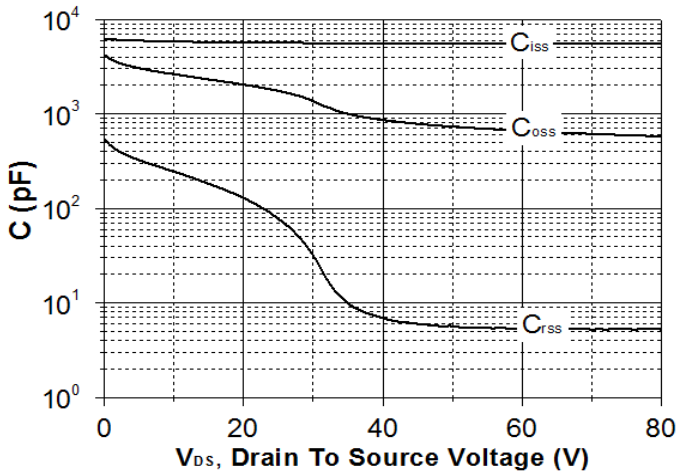


Figure3. Capacitance Characteristics

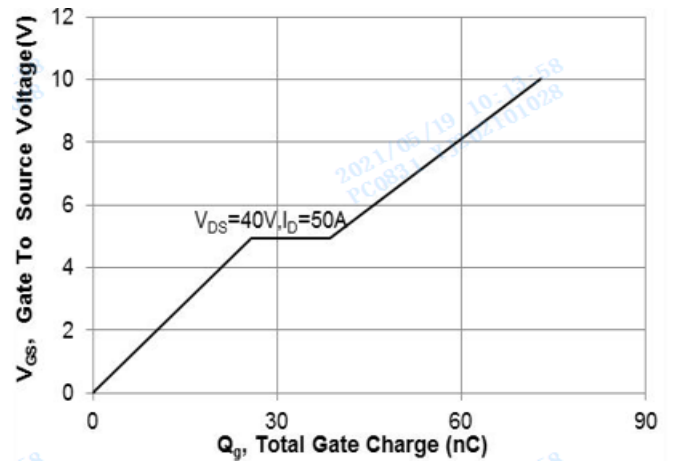


Figure4. Gate Charge

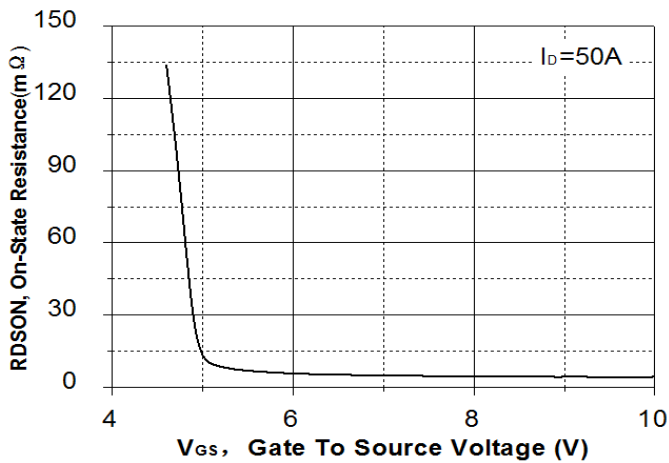


Figure5. On-Resistance vs. Gate to Source Voltage

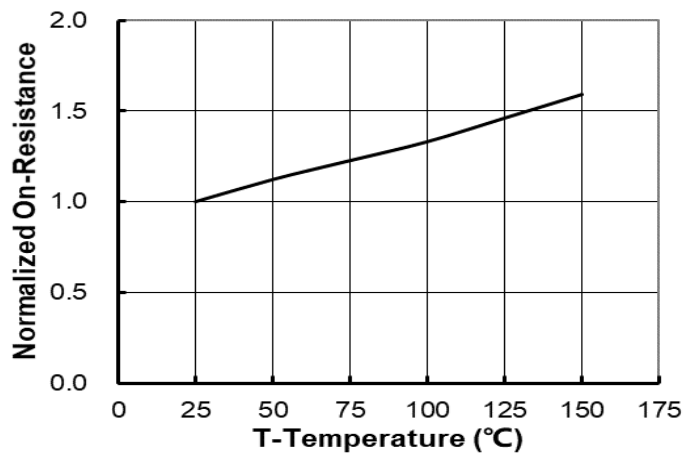


Figure6. Normalized On-Resistance



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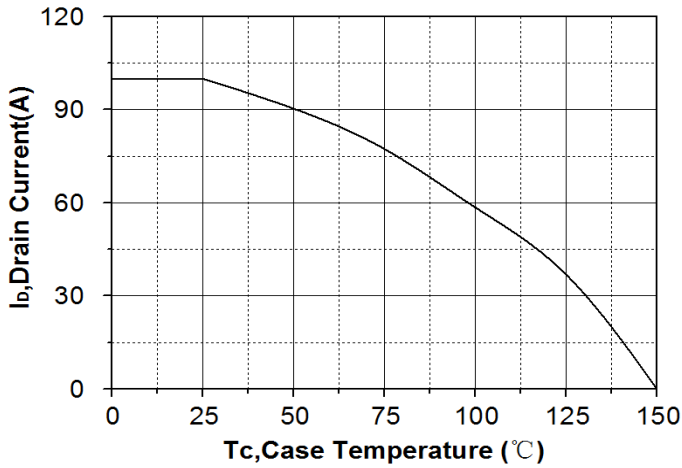


Figure7. Drain current

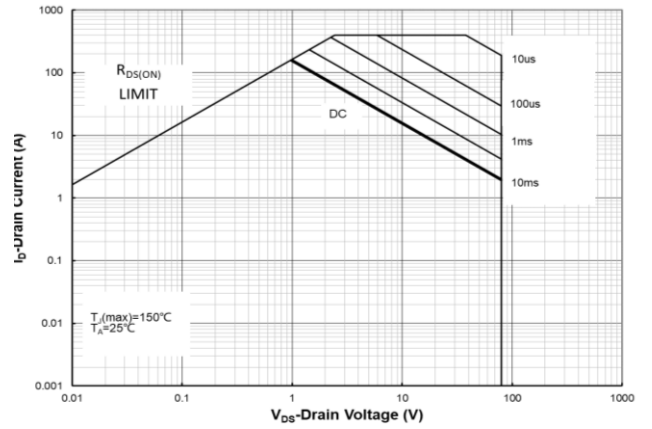


Figure8. Safe Operation Area

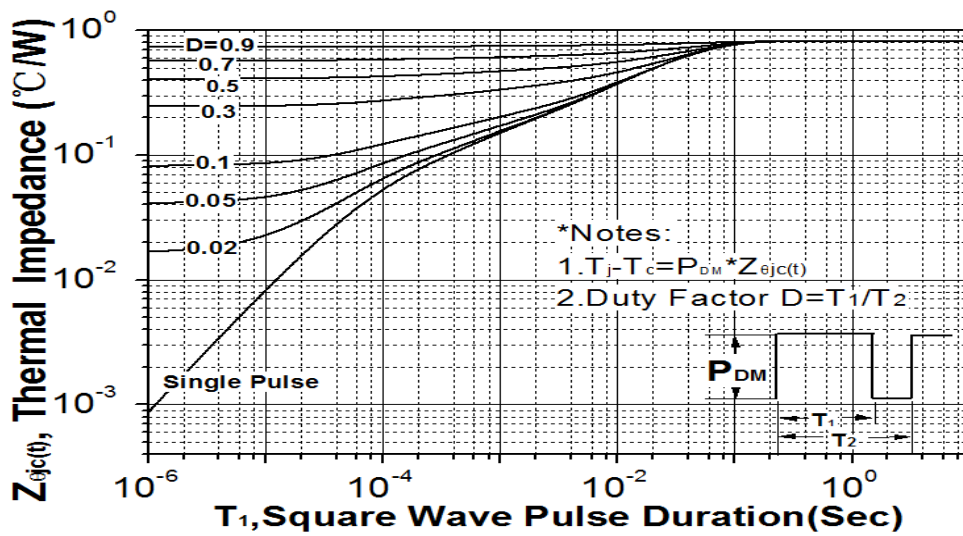
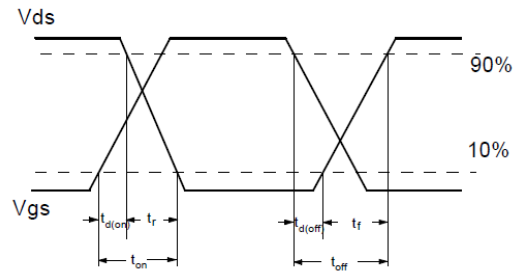
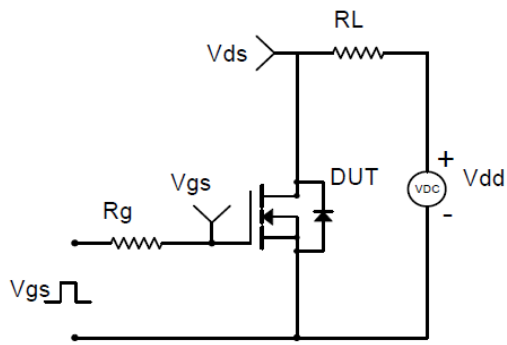
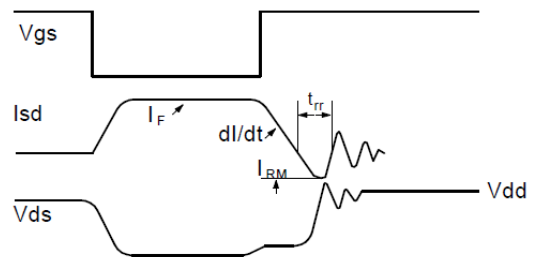
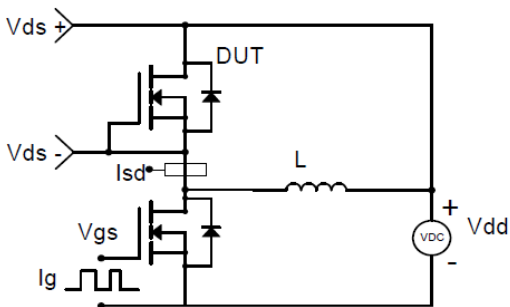


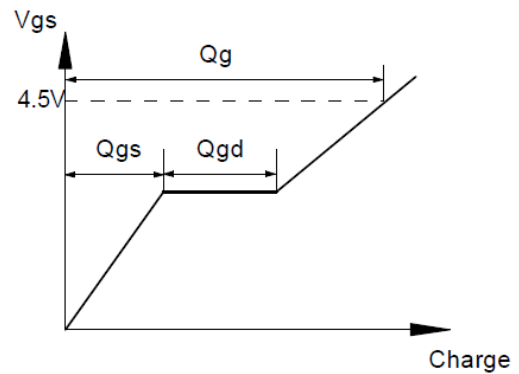
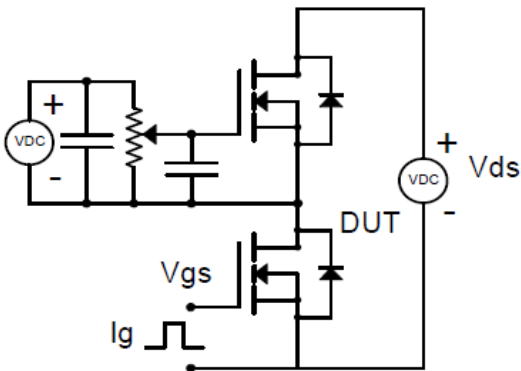
Figure9. Normalized Maximum Transient thermal impedance



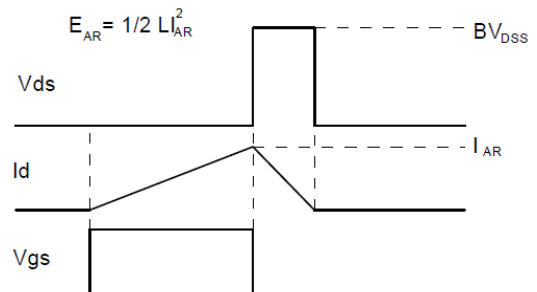
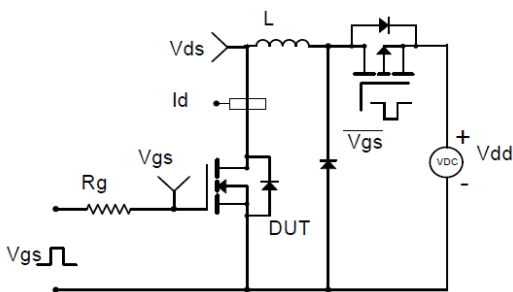
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

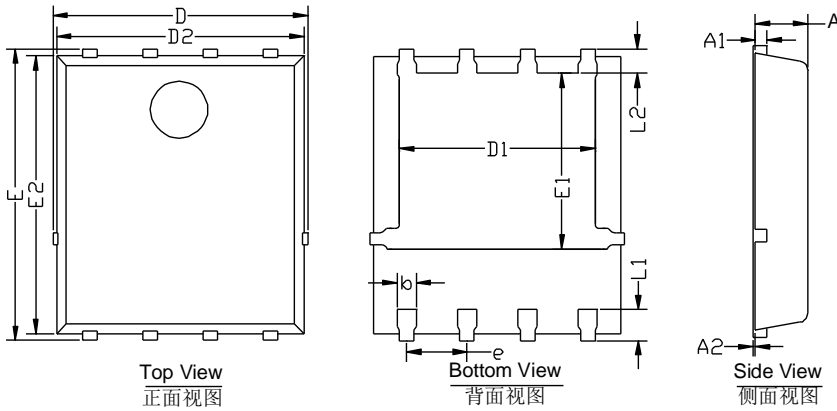


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

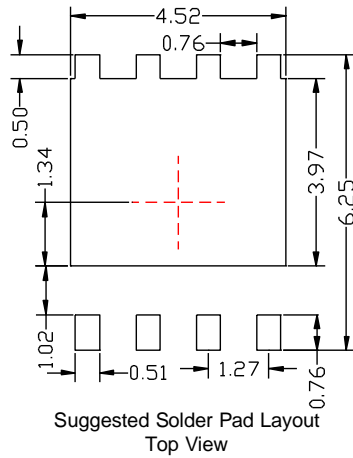


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■ PDFN5060-8L Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.



YJG100G08A

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