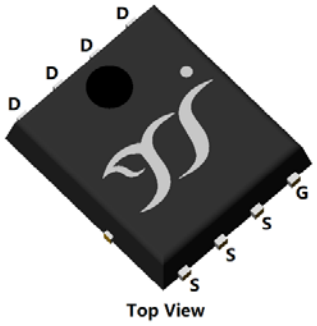
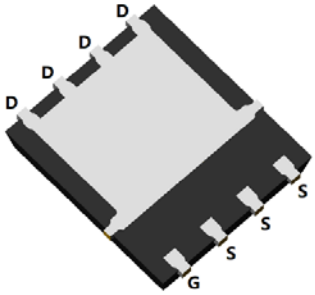
N-Channel Enhancement Mode Field Effect Transistor

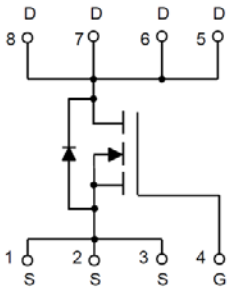


Top View



Bottom View

PDFN5060-8L



Product Summary

- V_{DS} 120V
- I_D 88A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜7.6mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜9.6mohm
- 100% UIS Tested
- 100% ▽VDS Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	120	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	88	A
	Tc=100℃		56	
Pulsed Drain Current [A]		I_{DM}	352	A
Avalanche energy [B]		EAS	400	mJ
Total Power Dissipation [C]	Tc=25℃	P_D	120	W
	Tc=100℃		48	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	15	20	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.84	1.04	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG88G12A	F1	YJG88G12A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	120	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	2.0	3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	6.4	7.6	mΩ
		V_{GS}=4.5V, I_D=20A	-	7.6	9.6	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V	-	-	1.3	V
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=20A	-	80	-	S
Gate resistance	R_G	f=1MHz, Open drain	-	0.9	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	88	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ	-	4619	-	pF
Output Capacitance	C_{oss}		-	924	-	
Reverse Transfer Capacitance	C_{rss}		-	28	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=20A	-	72.0	-	nC
Gate-Source Charge	Q_{gs}		-	19.5	-	
Gate-Drain Charge	Q_{gd}		-	8.2	-	
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us	-	195	-	
Reverse Recovery Time	t_{rr}		-	86	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,I_D=20A R_{GEN}=2.2Ω	-	19	-	
Turn-on Rise Time	t_r		-	36	-	
Turn-off Delay Time	$t_{D(off)}$		-	45	-	
Turn-off fall Time	t_f		-	45	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25℃, V_{DD}=50V, V_G=10V, R_G=25Ω, L=2mH,I_{AS}=20A

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation PDSM is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

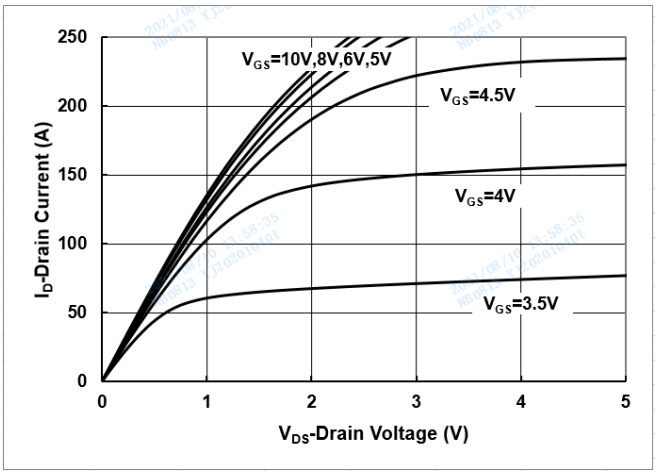


Figure1. Output Characteristics

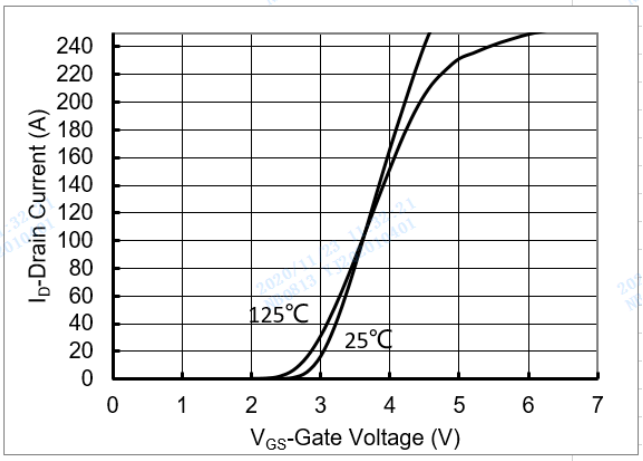


Figure2. Transfer Characteristics

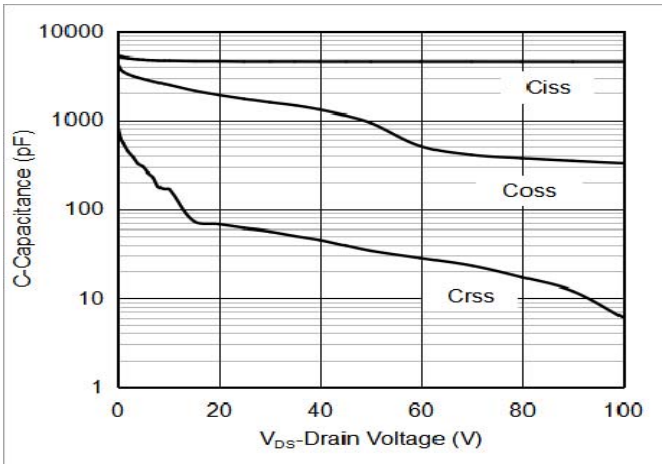


Figure3. Capacitance Characteristics

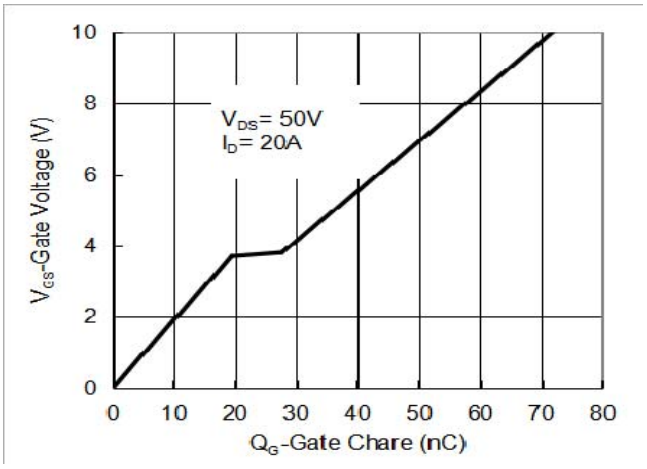


Figure4. Gate Charge

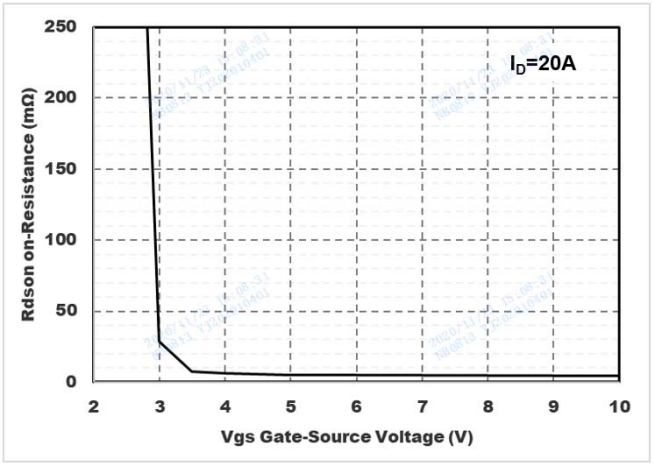


Figure5. : On-Resistance vs. Gate to Source Voltage

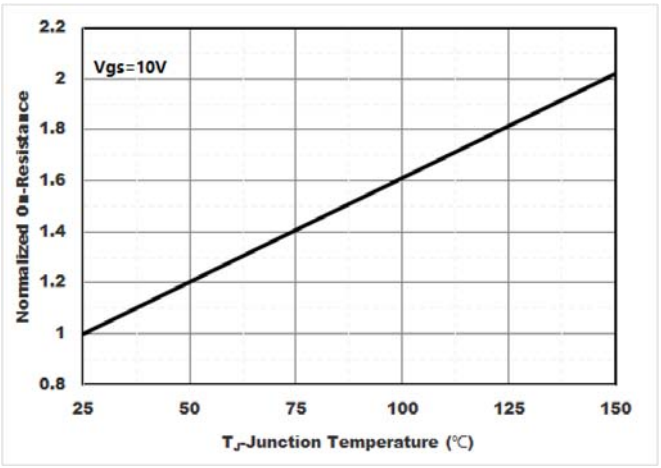


Figure6.Normalized On-Resistance

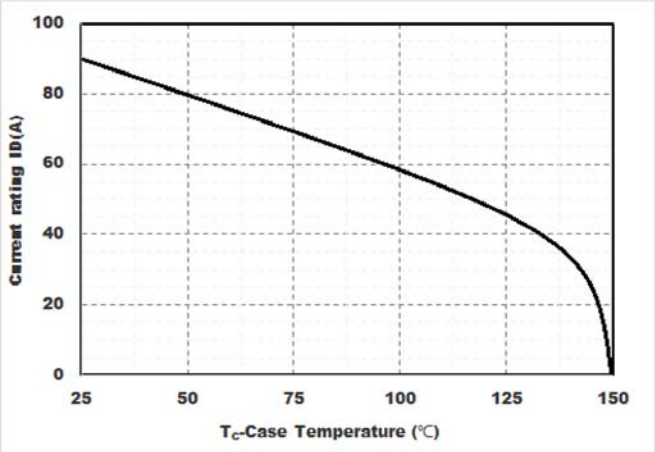


Figure7. Drain current

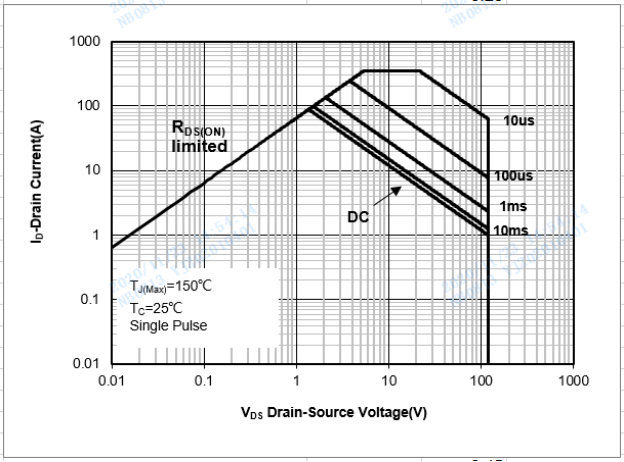


Figure8.Safe Operation Area

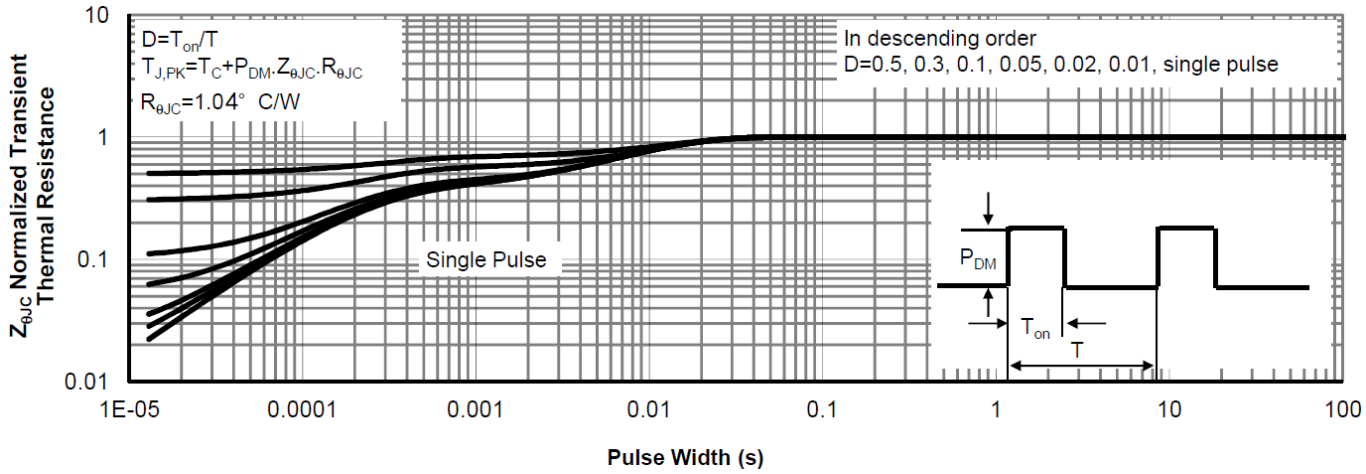
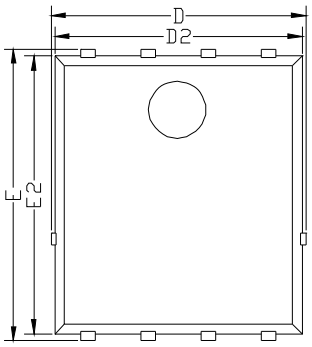
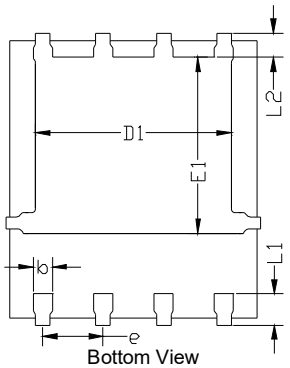


Figure9. Normalized Maximum Transient thermal impedance

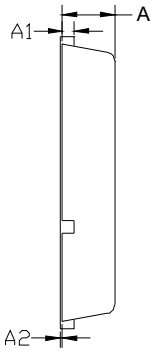
■ PDFN5060-8L Package information



Top View
正面视图



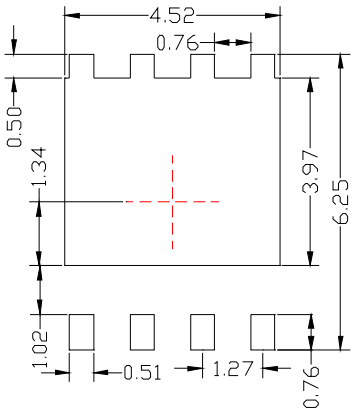
Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

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REV.	EFFECTIVE DATE	REVISION HISTORY	PREPARED
1.0	2020.11.23	New release	Ting Liu
2.0	2021.07.21	更新Ron,Cg and Switching Parameters以及output,Cg和Qg曲线	Ting Liu
2.1	2021.12.22	增加HF、MSL等级和UL等级，更新POD图和外形示意图，增加EAS的测试电流	Yunliang Lu